Amendment
Please amend claims 5, 7, 8, 9, 11, 13, 15 as shown.
Please cancel claim 10.
If the claims 1-3, 7-9, 11-14 are considered not allowable in view of the amendment, they shall be cancelled.

Remarks

Rejection under 35 USC 112

Claim 5 has been amended to read "The method of Claim 4".
Claims 5 and 6 therefore now correctly depend from claim 4.

Claim 7 was rejected for indefiniteness since GGNMOS is an indefinite reference point. It is respectfully submitted that a GGNMOS device (Grounded gate N-type metal oxide semiconductor) is a structure that is well known in the art. Furthermore, it is common practice to distinguish between components by referring to their characteristics or specifications. In this case, the particularities of the GGNMOS are clearly defined by referring to its characteristics, namely a GGNMOS having the **same holding voltage**. Thus both the structure (GGNMOS - which is well known in the art) as well as the particular parameters are clearly defined. Inherent in the claim is the fact that we are comparing apples to apples, or, in this case, structures that are otherwise the same, e.g., made by the same process, e.g., using 0.18um process. Thus it is respectfully submitted that the claim is definite as it stands. However, for additional clarity, the structure of a conventional GGNMOS is included in the claim.

Claim 7 was also argued to be indefinite since it referred to increasing the holding voltage to the desired level. As discussed in the response filed September 3, 2002 to the claim 4 rejection,(which was subsequently accepted) "the desired level" does not lack indefiniteness since the "desired" elevated holding voltage is the predetermined voltage chosen by the manufacturer to avoid latch-up. In the specification, one such "desired" voltage is given as a voltage that is above the DC bias, e.g., the power supply voltage, to avoid latch-up (page 5, second last paragraph, and page 11, lines 4-6. The size of the emitter is determined by TCAD simulations as discussed on page 9, first two lines. Thus the specification clearly explains how the size is chosen using TCAD simulations to achieve a holding voltage that avoids latch-up. Thus both the desired voltage and the manner of achieving it are clearly defined. Nevertheless, claim 7 was amended to use clearer wording.

Claim 8 was rejected for reasons similar to claim 7. It is respectfully submitted that the same arguments apply to claim 8. A GGNMOS is a well known structure, and by specifying the parameters, ie a GGNMOS with the same holding voltage, the claim is couched in clearly defined terms. Also, as mentioned with respect to claim 7, "the desired level" is a clearly defined term since it refers to the predefined level at which there is no latch-up. Again, however, the structure of a conventional GGNMOS is included in the claim.

Claim 8 was further rejected for reciting a p+ emitter that is reduced below "a predetermined value". Claim 8 has been amended to specify that the p+ emitter size is predefined and that the n+ emitter is then increased in size to achieve a predefined holding voltage level. The predefined size can be any size chosen by the manufacturer but clearly within a range that will allow the n+ emitter to be adjusted to achieve the desired holding voltage.

Claim 9 was rejected since LVTSCR and GGNMOS are indefinite reference points. It is respectfully submitted that both GGNMOS and LVTSCR structures are well known in the art and therefore structurally not indefinite. Also, the holding voltage of a LVTSCR and current capabilities of a GGNMOS can be clearly defined within a narrow range for a certain process. Inherent in the claim is that the device of the invention is compared to GGNMOS and LVTSCR devices made by the same process. However, to avoid argument on this point, claim 9 has been amended to specifically mention this. Also, the structures of a conventional GGNMOS and LVTSCR are included.

Claim 10 has been deleted.
Claim11 was rejected since it uses a conventional LVTSCR as a reference point. As discussed above, a LVTSCR device is a well known structure in the art, having a well defined range within which the holding voltage falls. Again claim 11 has been amended to explicitly state that we are referring to a LVTSCR of the same process. The claim was also amended to provide antecedent basis for the p+ emitter. Also, the structure of a conventional LVTSCR is included in the claim.

Claim 12 was rejected for depending from claim 11 and for referring to a "desired holding voltage". As discussed above with respect to claim 7, the desired holding voltage is definite since it is the predefined voltage that avoids latch-up.
In view of the amendment and the explanation above in response to the claim 7 and claim 11 rejections, it is respectfully submitted that claim 12 is also no longer indefinite.

Claim 13 was rejected for using a conventional GGNMOS as a reference point and because of lack of antecedent basis for p+ emitter. As mentioned above, a GGNMOS structure is well known in the art and has well defined current capabilities. Thus the reference to the current capabilities of a conventional GGNMOS, is in fact clearly understood by those skilled in the art. Furthermore, claim 13 has been amended to specify that the device is made by the same process as the GGNMOS to which it is compared, and to provide antecedent basis for the p+ emitter. Again, the claim was amended to include the structure of a conventional GGNMOS.

Claim 14 was rejected because "desired current" is indefinite. It is respectfully submitted that "desired current" refers to the current that is needed to withstand a particular ESD pulse level. Thus, it refers to a pre-defined value that is clearly defined. This current parameter is discussed in paragraph 4 of the Background of the Invention, in which it is stated that GGNMOS are not only large, they also support only limited current density. As mentioned, the ESD protection capabilities can be defined in terms of the required contact width of the structure required to protect against a particular ESD pulse amplitude.
It is therefore respectfully submitted that claim 14 is clearly defined and does not lack definiteness.

Claim 15 was rejected for lack of antecedent basis for the p+ emitter. Claim 15 has been amended to provide the antecedent basis for the p+ emitter as well as for the n+ emitter referred to in Claim 16.

Rejection under 35 USC 102 or 103

Claim 7 was rejected over Fig 1 of the prior art reference, and claims 8-16 were rejected over Figure 2 of the prior art reference.'

It is respectfully submitted that the claims are method claims that deal with adjusting of region sizes. This manipulation of region sizes is not taught or suggested by either Figure 1 or 2 of the cited reference. The p+ emitter and n+ emitter in Figures 1 and 2 of the prior art reference are merely depicted as static regions.

Version with markings to show changes made

5. (Amended) The method (device) of claim (2) 4, wherein the first conductivity type is p type and the second conductivity type is n type.

7. (Amended) A method of providing a device having a holding voltage substantially the same as a conventional GGNMOS, wherein the GGNMOS comprises a n+ drain and a n+ source formed in p-material to define a p-channel between them as provided by any conventional GGNMOS, but supporting current densities that are at least twice as high as for (a) any conventional GGNMOS of substantially the same holding voltage, comprising

providing a SCR-like structure having a p+ emitter (that is sufficiently reduced in size), and

sizing the emitter so as to (limit hole injection hole injection to the point where the space charge neutralization is so limited as to increase the) provide a holding voltage (to the desired) of a defined level.

8. (Amended) A method of providing a device having a holding voltage substantially the same as a conventional GGNMOS, wherein the GGNMOS comprises a n+ drain and a n+ source formed in p-material to define a p-channel between them as provided by any conventional GGNMOS, but supporting current densities that are at least twice as high as for (a) any conventional GGNMOS of substantially the same holding voltage, comprising

providing a LVTSCR-like structure having a p+ emitter (that is reduced in size below a predetermined value) and a n+ emitter,

predefining the size of the p+ emitter, and (having a n+ emitter that is increased in size to a point where the space charge neutralization is so limited as to increase the holding voltage to the desired level.)

increasing the size of the n+ emitter to achieve a predefined holding voltage.

9. (Twice Amended) A method of providing a device having a higher holding voltage than a conventional LVTSCR, wherein the LVTSCR includes a n-well in a p-material, with a n+ and a p+ region formed in the p-material, and a second n+ region and a p+ emitter formed in the n-well, and a floating n+ drain formed partly in the n-well and partly in the p-material, and a gate, and supporting a higher current than a conventional GGNMOS, wherein the GGNMOS comprises a n+ drain and a n+ source formed in p-material to define a p-channel between them as provided by any conventional GGNMOS, both made by the same process as the device, comprising providing a LVTSCR-like structure having a p+ emitter that is sufficiently reduced in size relative to a conventional LVTSCR so as to increase the holding voltage to a desired level that is higher than that of a conventional LVTSCR.

11. (Amended) A method of creating an ESD protection structure having a higher holding voltage than a conventional LVTSCR made by the same process, wherein the LVTSCR includes a n-well in a p-material, with a n+ region and a p+ region formed in the p-material, and a second n+ region and a p+ emitter formed in the n-well, and a floating n+ drain formed partly in the n-well and partly in the p-material, and a gate, comprising

providing a LVTSCR-like structure as for the conventional LVTSCR, which includes the p+ emitter, and

manipulating the size of the p+ emitter.

13. (Amended) A method of creating an ESD protection structure that supports a higher current than a conventional GGNMOS device made by the same process as the structure, ,wherein the GGNMOS comprises a n+ drain and a n+ source formed in p-material to define a p-channel between them as provided by any conventional GGNMOS, both made by the same process as the device, comprising

providing a LVTSCR-like structure which includes a n-well in a p-material, with a n+ region and a p+ region formed in the p-material, and a second n+ region and a p+ emitter formed in the n-well, and a floating n+ drain formed partly in the n-well and partly in the p-material, and a gate, p+ emitter, and

manipulating the size of the p+ emitter.

15. A method of varying the holding voltage of a LVTSCR, which includes p+ emitter and a n+ emitter, comprising

adjusting the size of the p+ emitter.

In view of the amendments and arguments presented above, it is respectfully requested that claims 4, 5, 6, 15, 16, 17, 18, as they now stand, be allowed.
Furthermore, if the changes to the other claims are acceptable, it is also respectfully requested that they also be permitted to proceed to allowance.

Respectfully Submitted,

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